Low Power Scheduling for High-Level Synthesis

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*Abstract*—This paper explains how low power scheduling is used for High-Level Synthesis . Scheduling is one of many stages for high-level synthesis. By using low power scheduling, switching activity is reduced which meet the time constraints. More details about scheduling are written in this paper, so that we clearly understand the benefits of low power scheduling for High-Level Synthesis. (*Abstract*)

Diagram

Description automatically generatedKeywords—component, formatting, style, styling, insert (key words)

# Introduction (*Heading 1*)

In this world full of advanced technology, microelectronics is very vital and act as a backbone to the development of software and hardware systems in recent decades. All inventions and innovations that are made by humans in the past are inspirations and the starting point to the more advanced technological changes today that produce a complex system. A complex system that full of design layers and architecture need years of effort to make a system become real and not just a stupid ideology from an optimist or idealist. Challenges and failures that come by, become a great lesson to create a great and reliable system for a very long time. All the hardworks in creating model and prototype must be must be appreciated because without this effort, the resulting system would have been full of errors and less reliability.   
 The real embedded system, integrated circuit IC and robot automation are example of hot topics that many developers and engineers discuss on how to improve the creation of new advanced technology. Design, Fabrication, Testing and Packaging are four stages in the creation of integrated circuit.

# High level synthesis

## Definition

High-level Synthesis is a translation process from behavioral description into a structural description. Scheduling, allocation and binding are three phases of High-Level Synthesis. The phases are randomly ordered based on design flow and are used to support decision making on design stage , namely size, performance and for this topic, we focus on power consumption that has become more and more important in recent years. When talking about power consumptions, it means that we wanted to optimize the usage of energy for a system so that it become more efficient. The main purpose of low power scheduling in High-Level Synthesis is to schedule operations while minimizing switching activity and select low power modules while meeting the time constraints.

## Fundamentals of High-Level Synthesis

As mentioned, the three phases are scheduling, allocation and binding. In scheduling phase, the time for operation to be executed is determined. The allocation phase determines how many instances of each resources are required and the binding or also well-known as assignment phase selects on what resource a computational operation will be run. Figures 1 shows design phases of the High-Level Synthesis.

Most of the time, the input for High-Level Synthesis is a control data flow graph, called CDFG.

# Power consumption and dissipation

In recent years, the demand of personal computing devices and wireless communications equipment has increased. As a result, there is a greater demand for low-power circuit design. Along with area and run-time, lowering power consumption has become one of the most essential criteria. There are some reasons why the consideration of low power is very strong :

- Increased demand of portable systems which require the battery life to be more long lasting. Laptops and mobile phones are the big picture for this issue.

- Thermal considerations which means that the cost of cooling and packaging would be reduced if low power dissipation

-Environmental issues because when smaller power is dissipated, lower the heat pumped into the rooms which means that usage of electricity is reduced, hence give less impact on environment

The source of power consumption or dissipation in digital CMOS circuit are as shown in figure below:

Diagram

Description automatically generated.

The parameters that are independent and not related to each other to affect power consumption as well as energy usage are:

- supply voltage

-the clock frequency

-the switching activity per clock cycle at various signals in the circuit.

-the parasitic capacitance

Text

Description automatically generated with low confidenceThe parameters above are proven by an expression, called dynamic power dissipation expression.

CL is the load capacitor, Vdd is the supply voltage,αis the average or expected number of transitions per clock cycle also known as the switching activity, and f is the clock frequency

Hence, to optimize the power consumptions, the factors must be tackled. Here are the suggestions or ideas:

- using the smallest possible supply voltage.

- parallelism and pipelining mechanism to lower required frequency operation.

- power control by disconnecting the power source when the system is in idle mode.

# Scheduling algorithms in high-Level synthesis

Table

Description automatically generated with medium confidenceScheduling is one of the phases in High-Level Synthesis.

## Scheduling Algorithm with Multiple Supply Voltage

Define abbreviations and acronyms the first time they are used in the text, even after they have been defined in the abstract. Abbreviations such as IEEE, SI, MKS, CGS, sc, dc, and rms do not have to be defined. Do not use abbreviations in the title or heads unless they are unavoidable.

## Scheduling Algorithm based on Frequency Variation

* Use either SI (MKS) or CGS as primary units. (SI units are encouraged.) English units may be used as secondary units (in parentheses). An exception would be the use of English units as identifiers in trade, such as “3.5-inch disk drive”.
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## Scheduling Algorithm based on Switching Activity

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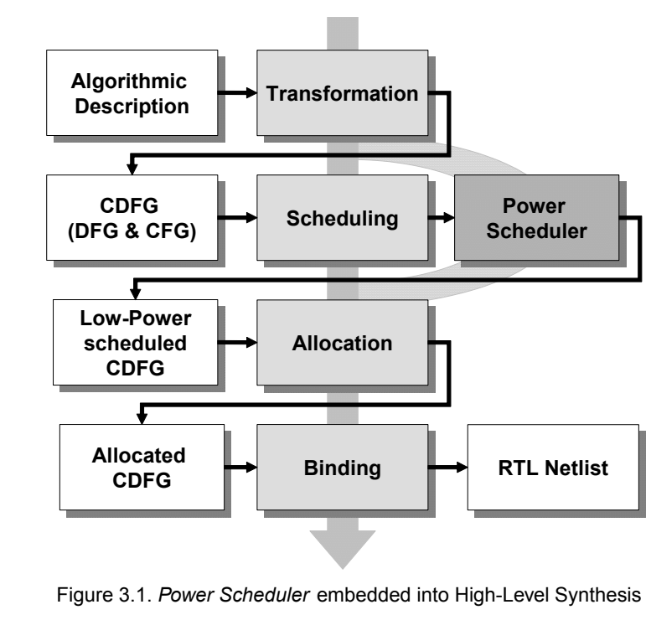
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# low power scheduling

The focus in this topic is how power consumption is optimized therefore low power is dissipated in scheduling task in High-Level Synthesis. The growing use of battery-powered and often wireless portable systems is boosting demand for low-power IC and SoC technologies. Furthermore, users have come to expect more capability and longer battery life from such systems. A modern cellular phone, for example, might have capabilities like the ability to operate as a personal digital assistant, storing data such as photos and connecting to the Internet. Implementing a stable power network and limiting power dissipation have become key issues for design engineers in today's exceedingly big and complicated architectures.

## Methodology analysis

To integrate low power methods in High-Level Synthesis, we developed a system called Power Scheduler, which shows in figure below.

As shown in figure above, we can see the effect or impact of Power Scheduler in scheduling process. It replaces the existing scheduler of High-Level Synthesis system which causes low power consumption at scheduling process before entering allocation phase.The scheduled Control Data Flow Graph is generated which support low power. To generate the graph by using partition method, so that each partition can be activated or deactivated, while combining partitions to be run, hence minimizing the additional control components which causes less energy usage.

## Power reducton method

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## Design Example

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## Standard Scheduling

Sddsdfdsfdfdshfjfnjnfjksfjfkjsbfjskfksdfsnfkdnfknf

## Path Determination

Asghjasgdjasbdsavddsadmnbdn dmasbdnd

## Compatibility Graph

Sdsadnsakmdnsandkndasndkandlndkasnlsnd

## Clique Problem

Fnasjkfasnfasndlsaldmlasmdldas

## Experimental Result

Asjdnasmdksadkdmsandkndasda

## Summary

**ghjjhghjghjhfhfhfhfhgfh**

# conclusion

##### Affidavit *(Heading 5)*

The preferred spelling of the word “acknowledgment” in

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